Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

CLAIMS LISTING (all of pending claims 1-3, 10-25)

Claim 1 (*Previously Presented*): A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming a conductive first layer containing primarily silicon, the first layer being to provide one or more floating gates for the nonvolatile memory;

(b) nitriding a silicon-containing surface of the first layer with a low temperature, low energy, surface nitriding process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said silicon-containing surface of the first layer at relatively low temperature and relatively low energy;

(c) subjecting the nitrided surface to a thermally oxidizing atmosphere so as to thereby form a thermally-grown silicon oxide at the nitrided surface, the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms defining at least part of a first dielectric of the nonvolatile memory; and

(d) forming a conductive second layer separated by the first dielectric from conductive material of the first layer, the conductive second layer providing one or more control gates for the nonvolatile memory.

Claim 2 (*Previously Presented*): The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises performing oxidation at a temperature in the range 800°C-1050°C in an oxygen or oxygen/hydrogen atmosphere to thereby form the silicon oxide by thermal oxidation.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claim 3 (*Original*): The method of Claim 1 wherein the surface of the first layer is a polysilicon surface.

Claims 4-9 (*Canceled*)

Claim 10 (*Previously Presented*): The method of Claim 1 wherein the nitriding step includes using a Remote Plasma Nitridation (RPN) process.

Claim 11 (*Previously Presented*): The method of Claim 1 wherein the nitriding step includes using a Decoupled Plasma Nitridation (DPN) process.

Claim 12 (*Previously Presented*): The method of Claim 1 wherein the nitriding step provides a concentration of nitrogen atoms of 1-20 atomic percent in the nitrided surface.

Claim 13 (*Previously Presented*): The method of Claim 12 wherein the nitriding step incorporates said nitrogen atoms to a depth of no more than 3 nm in said surface of the first layer.

Claim 14 (*Previously Presented*): The method of Claim 1 wherein said first layer is disposed over a tunneling dielectric.

Claim 15 (*Previously Presented*): The method of Claim 14 and further comprising: thermally growing the tunneling dielectric.

Claim 16 (*Previously Presented*): The method of Claim 1 and further comprising: depositing a silicon nitride layer on said combination of the thermally-grown silicon oxide and incorporated nitrogen atoms to thereby define a further part of the first dielectric of the nonvolatile memory.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claim 17 (*Previously Presented*): The method of Claim 16 and further comprising:

depositing a silicon oxide layer on said deposited silicon nitride layer to thereby define a yet further part of the first dielectric of the nonvolatile memory.

Claim 18 (*Previously Presented*): A method of manufacturing a nonvolatile memory cell within a monolithically integrated circuit, the method comprising:

(a) forming a tunneling dielectric layer on a semiconductive substrate;

(b) forming a floating gate layer on said tunneling dielectric layer, the floating gate layer having a top surface composed primarily of conductive silicon;

(c) surface nitridating said top surface of the floating gate layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said top surface of the floating gate layer at relatively low temperature and relatively low energy; and

(d) subjecting the nitrided top surface to a thermally oxidizing atmosphere so as to thereby form a combination of thermally-grown silicon oxide and surface incorporated and thermally treated nitrogen atoms at the nitrided and thermally oxidized top surface of the floating gate layer.

Claim 19 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further comprising:

(e) depositing a silicon nitride layer directly on the nitrided and thermally oxidized top surface of the floating gate layer.

Claim 20 (*Previously Presented*): The memory cell manufacturing method of Claim 19 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Claim 21 (*Previously Presented*): The memory cell manufacturing method of Claim 19 and further comprising:

(f) depositing a silicon oxide layer directly on the silicon nitride layer.

Claim 22 (*Previously Presented*): The memory cell manufacturing method of Claim 21 and further comprising:

(g) surface nitridating said deposited silicon oxide layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said deposited silicon oxide layer at relatively low temperature and relatively low energy.

Claim 23 (*Previously Presented*): The memory cell manufacturing method of Claim 22 and further comprising:

(h) forming a conductive gate layer on said surface nitridated and deposited silicon oxide layer.

Claim 24 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

Claim 25 (*Previously Presented*): The memory cell manufacturing method of Claim 18 and further wherein:

said surface nitridating step incorporates nitrogen atoms into the said top surface of the floating gate layer to a depth of less than 3nm.

***

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262